(Translation of a notice from the Japanese Patent Office)

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NOTIFICATION OF REASONS FOR REJECTION

Patent Application No.: 011164/98
Examiner's Notice Date: September 12, 2002
Examiner: Mr. Hidetada MATSUSHIMA
Attorney for Applicant: Mr. Takehiko Suzuye et al.

This application is rejected on the grounds stated below. Any opinion regarding this reason must be filed within SIXTY DAYS of the mailing date thereof.

REASONS

1. The inventions described in the following claims of the present application are unpatentable under Section 29(1)(iii) of the Patent Law as being described in the following publications distributed overseas or in Japan prior to this application.

2. The inventions described in the following claims of the present application are unpatentable under Section 29 (2) of the Patent Law, as being such that they could easily have been made by a person with ordinary skill in the art to which they pertain, on the basis of the inventions described in the following publications distributed in Japan or a foreign country prior to this application.

3. The application fails to satisfy the requirements under Section 36(4) of the Patent Law, on the grounds that the specification is defective in the following respects.

REMARKS

CLAIMS 1-4:

REASONS 1 and 2

Reference 1

Refer to FIG. 1 and its related explanations in Reference 1.

Reference 1 discloses executing a step of forming a low-concentration source region and a drain region and a step of forming a high-concentration source region and a high-concentration drain region by ion implantation at one

time (paragraph [0027]). Thus, positions where the impurity concentration is maximum in the direction of depth in the low concentration region and high concentration region correspond to each other at a connecting portion thereof.

CLAIMS 1 and 2:

REASONS 1 and 2

References 2 and 3

Refer to FIG. 1 and its explanations in Reference 2, and FIGS. 2 and 3 and their explanations in Reference 3.

In References 2 and 3, impurity for a high-concentration source-drain region and impurity for a low-concentration source-drain region are introduced simultaneously. Thus, positions where the impurity concentration is maximum in the direction of depth in the low-concentration source-drain region and high-concentration source-drain region correspond to each other at a connecting portion thereof.

CLAIMS 5 and 9:

REASONS 1 and 2

Reference 4

Refer to FIG. 1 and its explanations in Reference 4.

CLAIMS 10, 11 and 14:

REASON 2

Reference 4

Doping an only channel portion for adjustment of a threshold value and silicifying a gate electrode and a source-drain region for low resistance have been well-known techniques at the filing date of the present application.

In addition, selection of materials of the first, second and third insulation films is a matter of design which a person skilled in the art can arbitrarily accomplish.

CLAIMS 5, 9 and 10:

REASONS 1 and 2

Reference 5

Refer to FIGS. 5 and 6 and their explanations in Reference 5.

CLAIMS 11 and 14:

REASON 2

Reference 5

Silicifying a gate electrode and a source-drain region for low resistance has been a well-known technique at the filing date of the present application.

In addition, selection of materials of the first, second and third insulation films is a matter of design which a person skilled in the art can arbitrarily accomplish.

CLAIMS 5-14:

REASON 3

Claims 5 to 14 recite a method of manufacturing an MIS type field effect transistor having an extension region.

However, claims 5 to 14 do not describe that a position where the impurity concentration in the direction of depth of the extension region is maximum corresponds to a position where the impurity concentration in the direction of depth of the source-drain region is maximum, at their connecting portion. Thus, claims 5 to 14 recite even inventions wherein a position where

the impurity concentration in the direction of depth of the extension region is maximum does *not* correspond to a position where the impurity concentration in the direction of depth of the source-drain region is maximum, at their connecting portion. It is unclear how such inventions can be accomplished even if the Detailed Description of the Invention and the drawings of the present application are reviewed.

Therefore, the Detailed Description of the Invention is not described so clearly or sufficiently that a person skilled in the art cannot accomplish the inventions of claims 5 to 14.

As the manufacturing methods in claims 5 to 14 may not be considered to correspond to the method of manufacturing a semiconductor apparatus as described in claim 1, claims 5 to 14 may not satisfy the requirements under Section 37(3) of the Patent Law.

* CITED REFERENCES

1. Jpn. Pat. Appln. KOKAI Publication No. 05-283422
2. Jpn. Pat. Appln. KOKAI Publication No. 02-126681
3. Jpn. Pat. Appln. KOKAI Publication No. 06-061487
4. Jpn. Pat. Appln. KOKAI Publication No. 04-093080
5. Jpn. Pat. Appln. KOKAI Publication No. 07-106557

PRIOR ART SEARCH REPORT

*Searched Technical Fields:

NOTIFICATION OF REASONS FOR REJECTION

IPC 7th edition, H01L29/78

H01L21/336

*Prior-Art Documents:

Jpn. Pat. Appln. KOKAI Publication No. 63-127570

This record of prior art search report does not constitute the reason for rejection.